OPTIMIZATION OF CELL SUBTYPES IN A HIERARCHICAL DESIGN FLOW

ABSTRACT OF THE DISCLOSURE

Methods and apparatus are described for facilitating physical synthesis of a circuit design. The circuit design includes a plurality cell instances organized hierarchically. Each cell instance corresponds schematically to one of a plurality of cell types. Transistors in each of the cell instances is sized with reference to an objective function thereby resulting in a first plurality of cell subtypes for each cell type. Each cell subtype corresponding to a particular cell type differs from all other cell subtypes corresponding to the particular cell type by at least one transistor dimension. Selected ones of the subtypes for at least one of the cell types are merged thereby resulting in a second plurality of subtypes for the at least one of the cell types. The second plurality of subtypes being fewer than the first plurality of subtypes. The merging of the selected subtypes achieves a balance between the objective function and a cost associated with maintaining the selected subtypes distinct.